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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,053	11/16/2001	Tiangong Liu	79569-1 /jlo	7852

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DOWELL & DOWELL PC
2111 Eisenhower Ave.
Suite 406
Alexandria, VA 22314

EXAMINER	
PHAN, HANH	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,053	LIU ET AL.	
	Examiner	Art Unit	
	Hanh Phan	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-6, 17 and 18 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No. 10/024,303 (Lee et al). Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations recited in claims 1-6, 17 and 18 of the instant application are encompassed by claims 1-18 of copending Application No. 10/024,303 (Lee et al).

Regarding claims 1, 17 and 18, Lee et al (copending Application No. 10/024,303) discloses an integrated optical time division multiplexing (OTDM) module comprising:

an integrated modulator chip for generating at least first and second optical RZ signal streams; and

an integrated time-delay chip coupled to the integrated modulator chip for introducing a prescribed optical delay between said at least first and second optical RZ signal streams and for combining said at least first and second optical RZ signal streams after introduction of the prescribed delay (see claims 1-8 and 18 of copending Application No. 10/024,303).

Regarding claim 2, Lee et al discloses wherein the integrated modulator chip is a twin-modulator chip (see claims 1 and 18 of copending Application No. 10/024,303).

Regarding claim 3, Lee et al discloses wherein the integrated time-delay chip introduces a fixed optical time delay between said first and second optical RZ signal streams (see claims 1 and 18 of copending Application No. 10/024,303).

Regarding claim 4, Lee et al discloses wherein the integrated time-delay chip introduces a tuneable optical time delay between said first and second optical RZ signal streams (see claims 1 and 18 of copending Application No. 10/024,303).

Regarding claim 5, Lee et al discloses wherein the time-delay chip comprises first and second waveguides for receiving said first and second optical RZ signal streams from said integrated modulator chip, one of said first and second waveguides being of greater length than other of said first and second waveguides and both first and second waveguides being integrated within the fixed delay chip (see claim 1 of copending Application No. 10/024,303).

Regarding claim 6, Lee et al discloses wherein an electrode is deposited over a portion of said first or second waveguide of the time-delay chip that is greater in length, wherein a voltage applied to the electrode is used for fine tuning the optical time delay

introduced by the time-delay chip (see claim 11 of copending Application No. 10/024,303).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 3, 5, 12 and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Farries et al (US Patent No. 6,607,313).

Regarding claims 1, 17 and 18, referring to figures 4, 7 and 8, Farries teaches an integrated optical time division multiplexing (OTDM) module (i.e., an integrated micro-optic circuit having a slab waveguide chip 10, Fig. 4) comprising:

an integrated modulator chip (i.e., an integrated micro-optic circuit having a slab waveguide chip 10, Fig. 4) for generating at least first and second optical RZ signal streams; and

an integrated time-delay chip (i.e., spacer of glass 17, spacer of silicon 18 and birefringent crystal 14, Figs. 7 and 8) coupled to the integrated modulator chip for introducing a prescribed optical delay between the at least first and second optical RZ

signal streams and for combining the at least first and second optical RZ signal streams after introduction of the prescribed delay (col. 5, lines 40-67 and col. 6, lines 1-60).

Regarding claim 2, Farries further teaches wherein the integrated modulator chip (10)(Fig. 4) is a twin-modulator chip.

Regarding claim 3, Farries further teaches wherein the integrated time-delay chip (10)(Figs. 4, 7 and 8) introduces a fixed optical time delay between the first and second optical RZ signal streams.

Regarding claim 5, Farries further teaches wherein the time-delay chip comprises first and second waveguides for receiving the first and second optical RZ signal streams from the integrated modulator chip, one of said first and second waveguides being of greater length than other of the first and second waveguides and both first and second waveguides being integrated within the fixed delay chip (Figs. 4, 7 and 8, col. 6, lines 30-60).

Regarding claim 12, Farries further teaches wherein collimating lenses 9i.e., GRIN lenes 50a and 50b, Figs. 4 and 7) are used to couple the integrated modulator chip to the integrated time-delay chip.

Regarding claims 15 and 16, Farries teaches all the aspects of the claimed invention as set forth in the rejection claim 1 above. Farries further teaches a first and second variable optical attenuators (see col. 5, lines 54-56).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farries et al (US Patent No. 6,607,313) in view of Epworth (US Patent No. 6,271,952).

Regarding claim 4, Farries differs from claim 4 in that he fails to teach a tuneable optical time delay. However, Epworth teaches a tuneable optical time delay (Fig. 9, col. 9, lines 6-16). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the tuneable optical time delay as taught by Epworth in the system of Farries. One of ordinary skill in the art would have been motivated to do this since Epworth suggests in column 9, lines 6-26 that using such a tunable optical time delay has advantage of allowing the total optical path difference between the two optical signal streams can be compensated and allowing for proper interleaving.

Regarding claim 6, the combination of Farries and Epworth teaches an electrode is deposited over a portion of said first or second waveguide of the time-delay chip that is greater in length, wherein a voltage applied to the electrode is used for fine tuning the optical time delay introduced by the time-delay chip (see Fig. 9 of Epworth, col. 9, lines 6-16).

7. Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farries et al (US Patent No. 6,607,313) in view of Vaerewyck (US Patent No. 4,768,848).

Regarding claims 7 and 8, Farries differs from claims 7 and 8 in that he fails to teach an epoxy is used to couple optically and mechanically the integrated modulator chip to the integrated time-delay chip. However, Vaerewyck teaches an epoxy is used to couple optically and mechanically the optical fiber 22 and waveguide 14 (Fig. 1, col. 4, lines 25-37). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the epoxy as taught by Vaerewyck in the system of Farries. One of ordinary skill in the art would have been motivated to do this since Vaerewyck suggests in column 4, lines 25-37 that using such an epoxy has advantage of allowing coupling two optical devices together and improving the optical coupling efficiency.

Regarding claims 9-11, the combination of Farries and Vaerewyck teaches the epoxy has a refractive index n, the integrated modulator chip has a refractive index n1, the integrated time-delay chip has a refractive index n2 and wherein the refractive index n of the epoxy is defined by $n1<n<n2$ (col. 4 of Vaerewyck, lines 25-37).

Regarding claim 14, Farries teaches all the aspects of the claimed invention as set forth in the rejection claim 1 above. Farries further teaches a first and second variable optical attenuators (see col. 5, lines 54-56).

Farries differs from claim 14 in that he fails to teach an epoxy is used to couple optically and mechanically the integrated modulator chip to the integrated time-delay chip. However, Vaerewyck teaches an epoxy is used to couple optically and mechanically the optical fiber 22 and waveguide 14 (Fig. 1, col. 4, lines 25-37). Therefore, it would have been obvious to one having skill in the art at the time the

invention was made to incorporate the epoxy as taught by Vaerewyck in the system of Farries. One of ordinary skill in the art would have been motivated to do this since Vaerewyck suggests in column 4, lines 25-37 that using such an epoxy has advantage of allowing coupling two optical devices together and improving the optical coupling efficiency.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farries et al (US Patent No. 6,607,313) in view of Bergano et al (US Patent No. 5,111,322).

Regarding claim 13, Farries differs from claim 13 in that he fails to teach the prescribed optical delay introduced between the first and second optical RZ signal streams is approximately one half the period of each of first and second optical RZ signal streams. However, Bergano teaches the prescribed optical delay introduced between the first and second optical signal streams is approximately one half the period of each of first and second optical signal streams (Fig. 2, col. 3, lines 10-31). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the optical delay introduced between the first and second optical signal streams is approximately one half the period of each of first and second optical signal stream as taught by Bergano in the system of Farries. One of ordinary skill in the art would have been motivated to do this since Bergano suggests in column 3, lines 10-31 that using such the optical delay introduced between the first and second optical signal streams is approximately one half the period of each of first and second optical

signal streams have advantage of allowing the two pulse streams are interleaved in time.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hanh Phan whose telephone number is (571)272-3035.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

Hanh Phan

Primary Examiner

11/12/2004